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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,164	06/28/2003	Leonard J Gardecki	BUR920030026US1	1163

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EXAMINER
KEBEDE, BROOK

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,164	GARDECKI ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *25-28* is/are withdrawn from consideration.

5)☒ Claim(s) *12-24* is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicants' election with traverse of the Group I invention, claim(s) 1-24 in the response filed on August 27, 2004, is acknowledged. The traversal is on the ground(s) that "the subject matter of all claims 1-28 is sufficiently related that all claims 1-28 is sufficiently related that through search for the subject matter of any one group of claims would encompass a search for the subject matter of the remaining claims..." This is not found persuasive.

A restriction requirement between one set of apparatus claims and a set of process claims was issued in the Office action of August 20, 2004. "Section 121 [of Title 35 USC] permits a restriction for 'independent and distinct inventions,' which the PTO construes to mean that the sets of claims must be drawn to separately patentable inventions." See *Applied Materials Inc. v. Advanced Semiconductor Materials* 40 USPQ2d 1481, 1492 (Fed. Cir 1996)(Archer, C.J., concurring in-part and dissenting in-part). An apparatus and the process of making the product using the apparatus are "two independent, albeit related inventions." See *In re Taylor*, 149 USPQ 615, 617 (CCPA 1966). "When two sets of claims filed in the same application are patentably distinct or represent independent inventions, the examiner is to issue a restriction requirement." See *In re Berg*, 46 USPQ2d 1226, 1233 n.10 (Fed. Cir. 1998).

The examiner, in issuing a restriction requirement, must demonstrate "one way distinctiveness." *Applied Materials Inc.* at 1492. As stated within the restriction requirement, "inventions are distinct if either or both of the following can be shown: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP §

806.05(e))." In this application, the examiner restricted the apparatus claims from the process claims on the grounds that "the apparatus of Group II can be used to hold wafer during CVD deposition of thin films on the wafer instead of forming bonding pads and solder bumps" and that, as a result, a restriction was necessary.

In addition to one-way distinctiveness, the examiner must show "why it would be a burden to examine both sets of claims." *Applied Materials Inc.* at 1492. "A serious burden on the examiner may be *prima facie* shown if the examiner shows by appropriate explanation either separate classification, separate status in the art, or a different field of search." MPEP 803. An explanation was provided in the restriction requirement. Specifically, in addition to being distinct, the examiner indicated that restriction is proper because the apparatus claims and the process claims "have acquired a separate status in the art."

The criteria of distinctness and burdensomeness have been met, as demonstrated hereinabove. Accordingly, the restriction requirement in this application is still deemed proper and is therefore **made FINAL**.

2. Claims 25-28 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention, the requirement having been traversed in the response filed on August 27, 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Shinogi et al. (US/6,534,387).

Re claim 1, Shinogi et al. disclose a method of forming a semiconductor interconnect comprising a first step of providing a semiconductor wafer (20) (see Fig. 8A); as second step of forming bonding pads (8) (see Fig. 8B) in a terminal wiring level on the front side of the wafer (20); a third step of reducing the thickness of the wafer (see Figs. 8C and 9A); a fourth step of forming solder bumps (12) (see Fig. 9B) on the bonding pads (8); and a fifth step of dicing the wafer into bumped semiconductor chips (see Fig. 9C).

Re claim 11, as applied to claim 1 above, Shinogi et al. disclose all the claimed limitations including the limitation annealing the solder bumps in order to reflow the solder bumps into semi-spherical shapes after the forming step of the solder bumps and before the dicing step (see Fig. 9B).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 2 and 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shinogi et al. (US/6,534,387) over Bhattacharya et al. (US/4,434,434).

Re claims, 2 and 4-9, as applied to claim 1 in Paragraph 4 above, Shinogi et al. disclose all the claimed limitations. However, Shinogi et al. do not specifically disclose the conventional process such as forming the solder bump through the evaporation mask that comprises molybdenum and forming of pad limiting metallurgy layer form materials selected from the group consisting of titanium nitride, copper, gold, titanium-tungsten, chrome, chrome-copper or combinations through the evaporation mask prior forming of the solder bump.

Bhattacharya et al. disclose a method of solder bump on the surface of the surface of the substrate that contains boding pads the method includes forming evaporation mask comprises molybdenum; forming pad limiting contact pad (i.e., pad limiting metallurgy layer) comprise chrome (Cr) or Cr/Cu through the evaporation mask; and forming the solder bump through the evaporation mask after forming of pad limiting metallurgy layer (see Col. 2, line 49 – Col. 5, line 5). As Bhattacharya et al. disclose, the process is utilized in order to provide novel solder mound limiting metallurgy which reduces cracking of brittle passivating coatings on semiconductor devices when solder mound terminals are formed (see Col. 1, lines 12-36).

Both Shinogi et al. and Bhattacharya et al. teachings are directed to forming a solder bumps to provide mechanical and electrical connection for semiconductor IC chips. Therefore, the teachings of Shinogi et al. and Bhattacharya et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Shinogi et al. reference with forming the solder bump through the evaporation mask that comprises molybdenum and forming of pad limiting metallurgy layer form materials selected from the group consisting of titanium nitride, copper, gold, titanium-tungsten, chrome, chrome-copper or combinations through the evaporation mask prior forming of the solder bump as taught by Bhattacharya et al. in order to provide novel solder mound limiting metallurgy which reduces cracking of brittle passivating coatings on semiconductor devices when solder mound terminals are formed.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shinogi et al. (US/6,534,387) in view of Miyamoto et al. (US/6,342,434).

Re claim 10, as applied to claim 1 in Paragraph 4 above, Shinogi et al. disclose grinding a backside of said wafer. However, Shinogi et al. dot not specifically disclose grinding process conducted with a rotating diamond grindstone, etching said backside surface of said wafer with a mixture of hydrofluoric and nitric acids while rotating said wafer, lapping the backside of said wafer by introducing a slurry containing abrasive particles between the backside of said wafer and a rotating wheel and, chemical-mechanical-polishing.

Miyamoto et al. disclose a conventional grinding process such as a rotating diamond grindstone, etching said backside surface of said wafer with a mixture of hydrofluoric and nitric acids while rotating said wafer, lapping the backside of said wafer by introducing a slurry

containing abrasive particles between the backside of said wafer and a rotating wheel and, chemical-mechanical-polishing to grind the rare surface of the wafer (i.e., back surface of the wafer) in order to thin the wafer.

Both Shinogi et al. and Miyamoto et al. teachings are directed to thinning the back surface of the wafer. Therefore, the teachings of Shinogi et al. and Miyamoto et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Shinogi et al. reference with conducting grinding process with a rotating diamond grindstone, etching said backside surface of said wafer with a mixture of hydrofluoric and nitric acids while rotating said wafer, lapping the backside of said wafer by introducing a slurry containing abrasive particles between the backside of said wafer and a rotating wheel and, chemical-mechanical-polishingas taught by Miyamoto et al. in order to thin the wafer.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shinogi et al. (US/6,534,387) over Bhattacharya et al. (US/4,434,434), as applied to claim 2 above in Paragraph 6 above, and further in view of Desai et al. (US/5,159,535).

Re claim 3, as applied to claim 2 in Paragraph 6 above, Shinogi et al. and Bhattacharya et al. in combination disclose all the claimed limitation including forming of a solder bump comprising a Pb-Sn alloy. However, both Shinogi et al. and Bhattacharya et al. do not specifically disclose the percentage composition of lead (Pb) and tin (Sn) alloy.

Desai et al. disclose forming of solder balls (i.e., solder bumps) composed of 95 % of lead (Pb) and 5% of tin (Sn) because the are thermally stable and relatively inexpensive to produce (see Col. 10, lines 3-48).

Shinogi et al., Bhattacharya et al., and Desai et al. teachings are directed to forming a solder bumps to provide mechanical and electrical connection for semiconductor IC chips. Therefore, the teachings of Shinogi et al., Bhattacharya et al., and Desai et al. are analogous.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Bhattacharya et al., reference with solder balls (i.e., solder bumps) composed of 95 % of lead (Pb) and 5% of tin (Sn) as taught by Desai et al. in order to thermally stable and relatively inexpensive solder bump.

Allowable Subject Matter

9. Claims 12-24 are allowed over prior art of record.

10. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art of record does not teach "providing an evaporation fixture comprising a bottom ring, a shim, an evaporation mask and a top ring; (e) placing said shim into said bottom ring; (f) placing said reduced thickness wafer on said shim; (g) placing on and aligning said mask to said reduced thickness wafer," as recited in claim 12.

Claims 13-24 are also allowed as being dependent of the allowed independent base claim.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Nye, III et al. (5,629,564), Rinne et al. (US/6,117,299), Costrini et al. (US/6,333,559), Tsuboi (US/6,528,881) also disclose similar inventive subject matter.

Correspondence

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Examiner
Art Unit 2823

BK
November 8, 2004